



# **MARITIME MIMO RADAR SYSTEM DESIGN CONSIDERATIONS**

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Dresden, 15.03.17

# OUTLINE

The RANGER project  
Primary FMCW MIMO principle  
Processing  
System architecture  
Conclusion

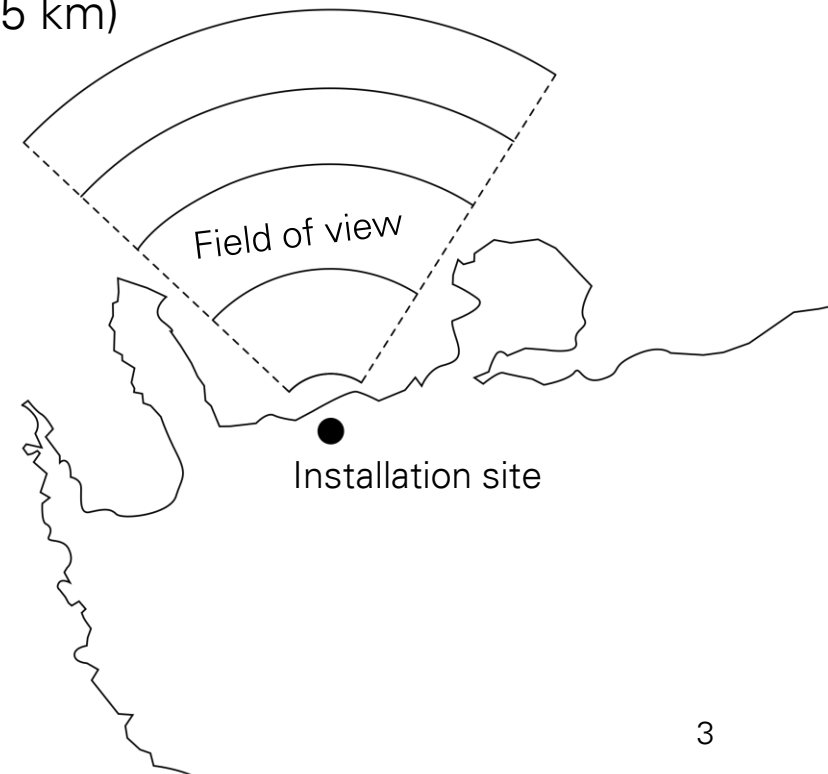
# RANGER PROJECT

## Maritime coastal radar

- OTH radar for distant targets (40-350 km)
- (PE-)MIMO radar for close targets (0-15 km)

## Tasks of TUD

- System evaluation of MIMO radar
- Design of radar frontend
- Design of output stage
- Antenna design
- Design of digital hardware
- Processing of raw data



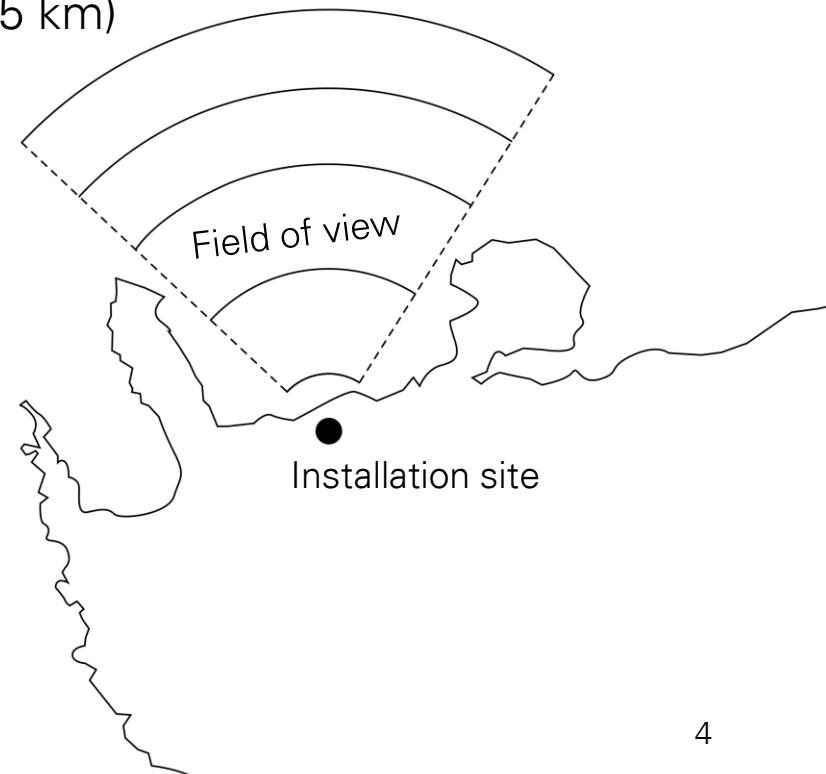
# RANGER PROJECT

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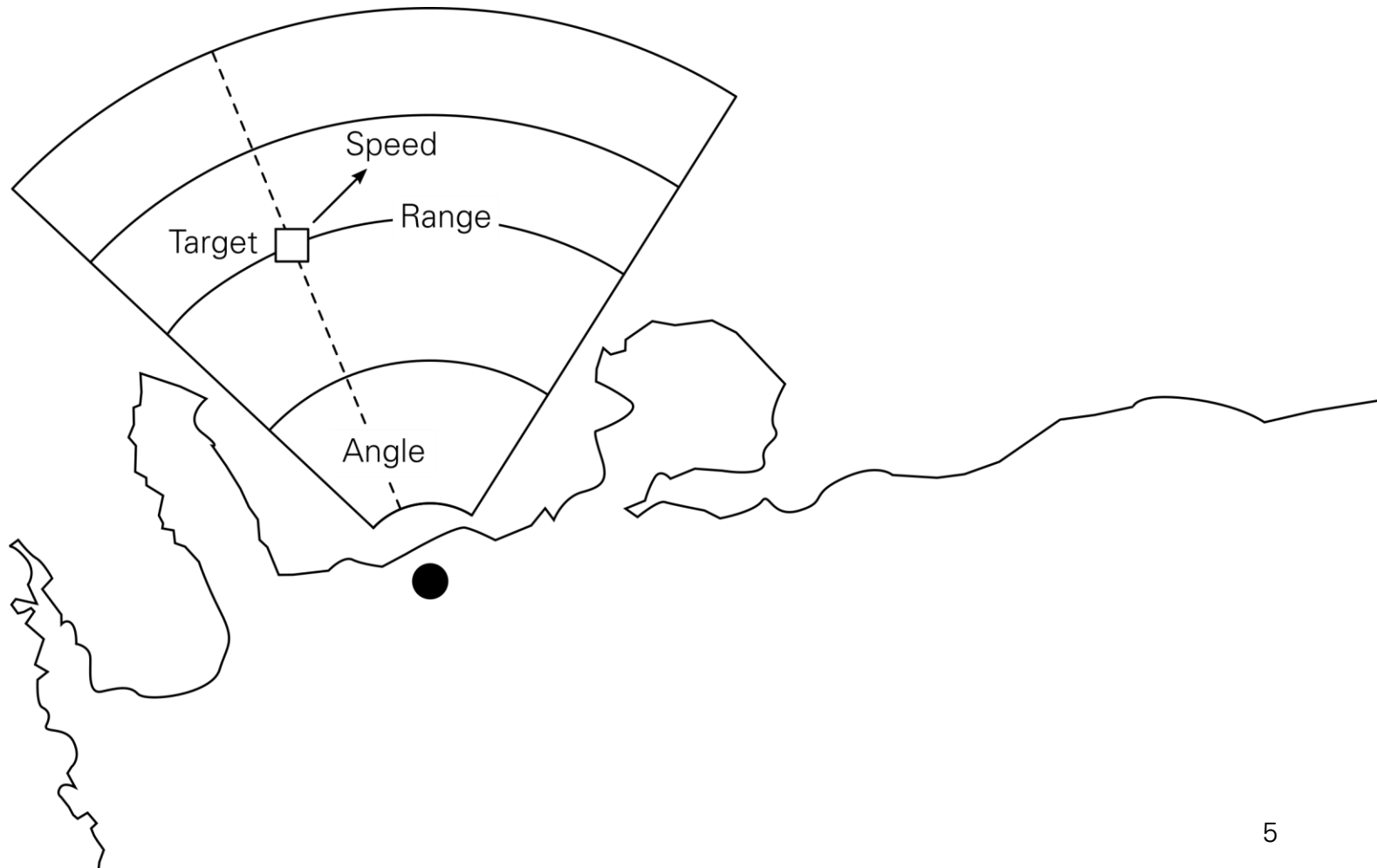
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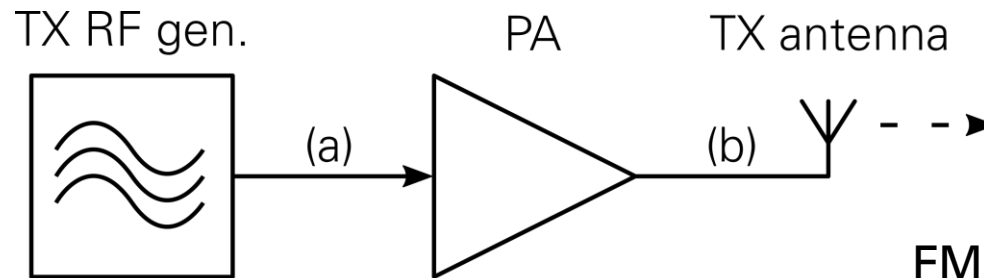
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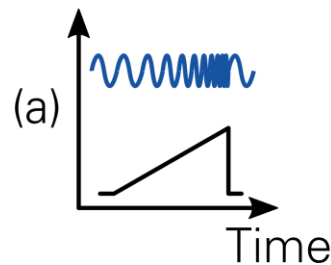
# RANGER PROJECT – PARAMETERS



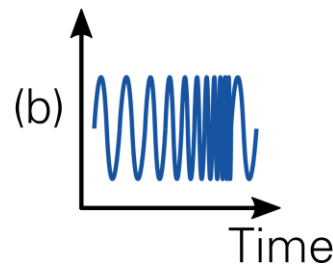
# FMCW BASICS – TRANSMISSION



Amplitude  
Frequency



Amplitude



## FMCW transmission

- PLL generates chirp waveform
- Amplification by power amplifier
- Transmission with antenna array

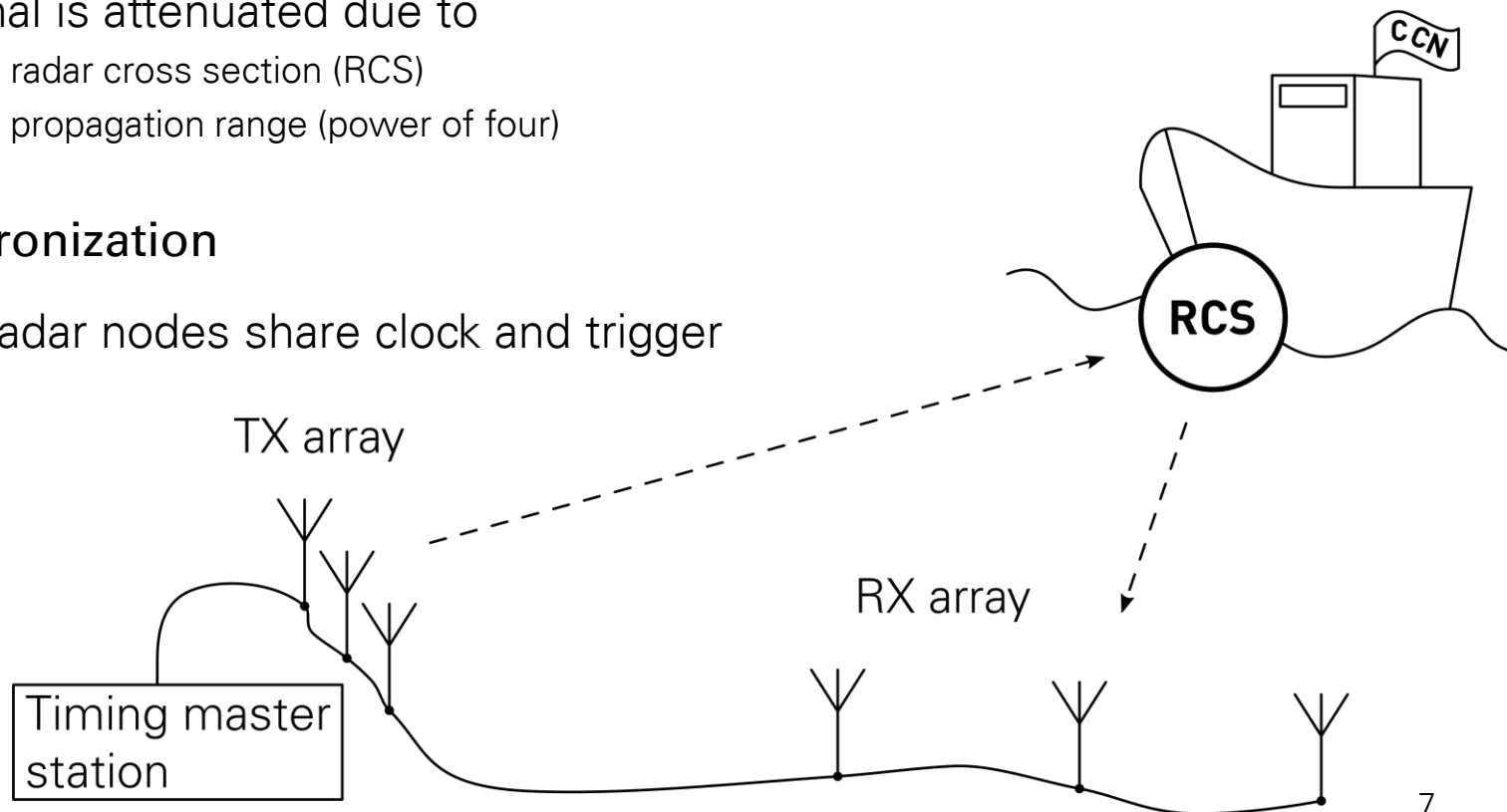
# FMCW BASICS – REFLECTION

## Attenuation

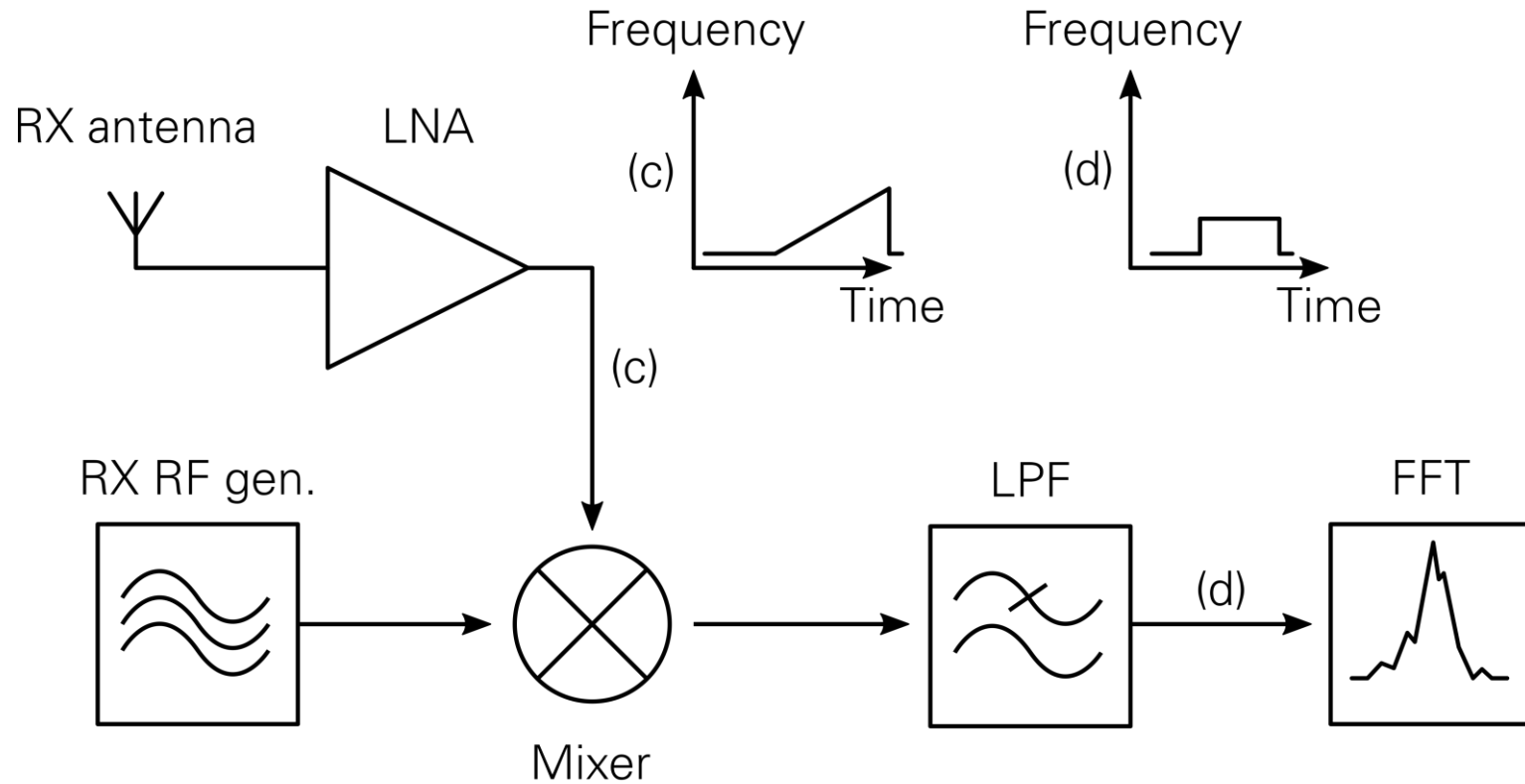
- Signal is attenuated due to
  - radar cross section (RCS)
  - propagation range (power of four)

## Synchronization

- All radar nodes share clock and trigger



# FMCW BASICS – RECEPTION

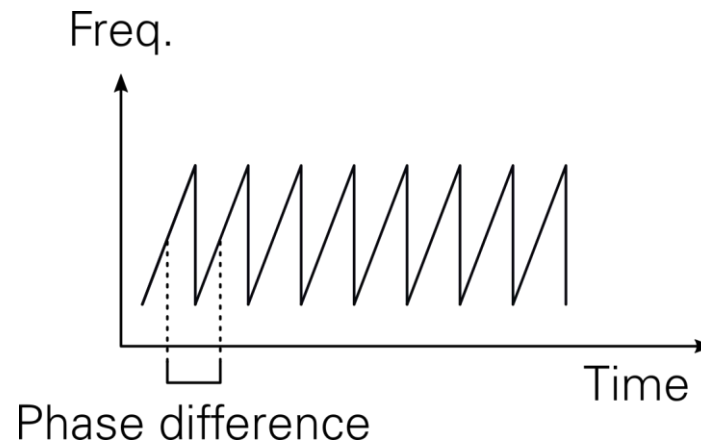




# PROCESSING – FOLLOWING STAGES

## Stage 2 – Velocity

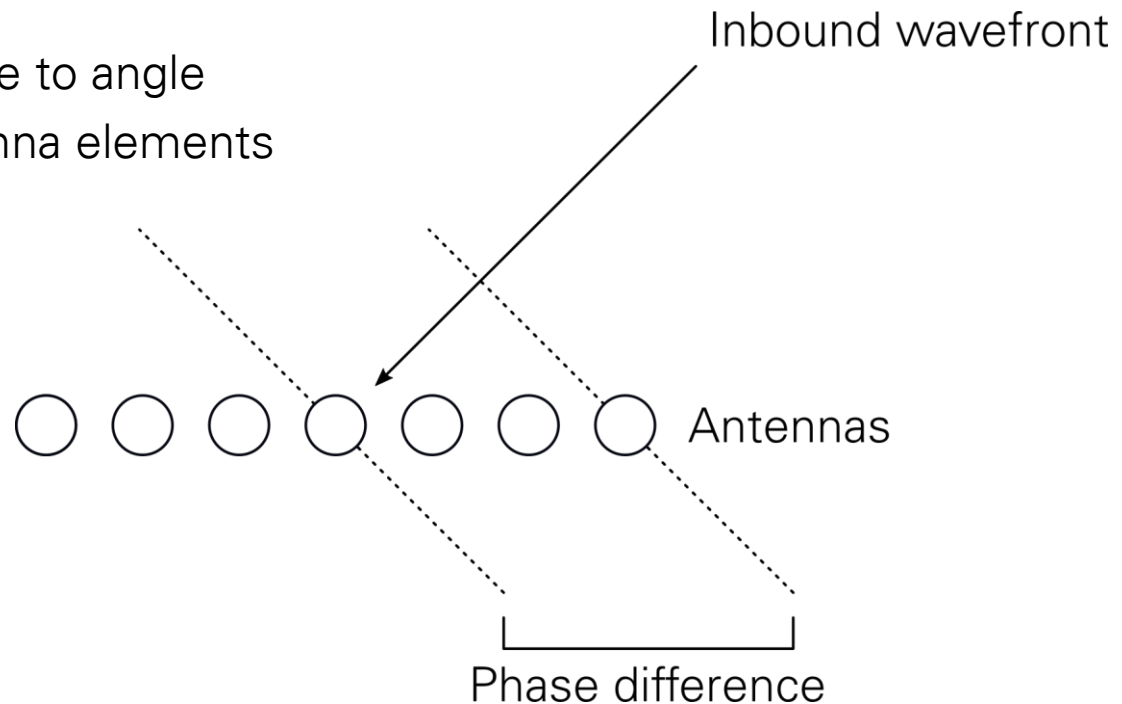
- Chirp sequence
- Phase shift translates to velocity
- FFTs on different chirps of a sequence at the same range bin



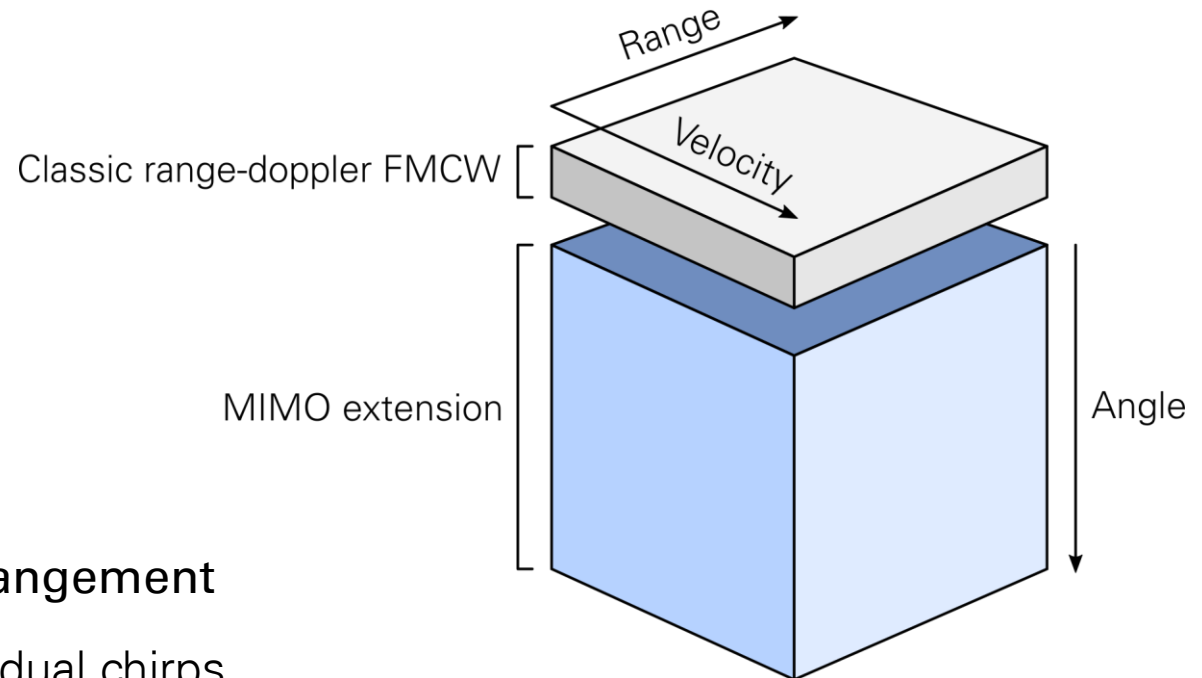
# PROCESSING – FOLLOWING STAGES

## Stage 3 – Angle

- MIMO array
- Phase shift due to angle
- FFT over antenna elements



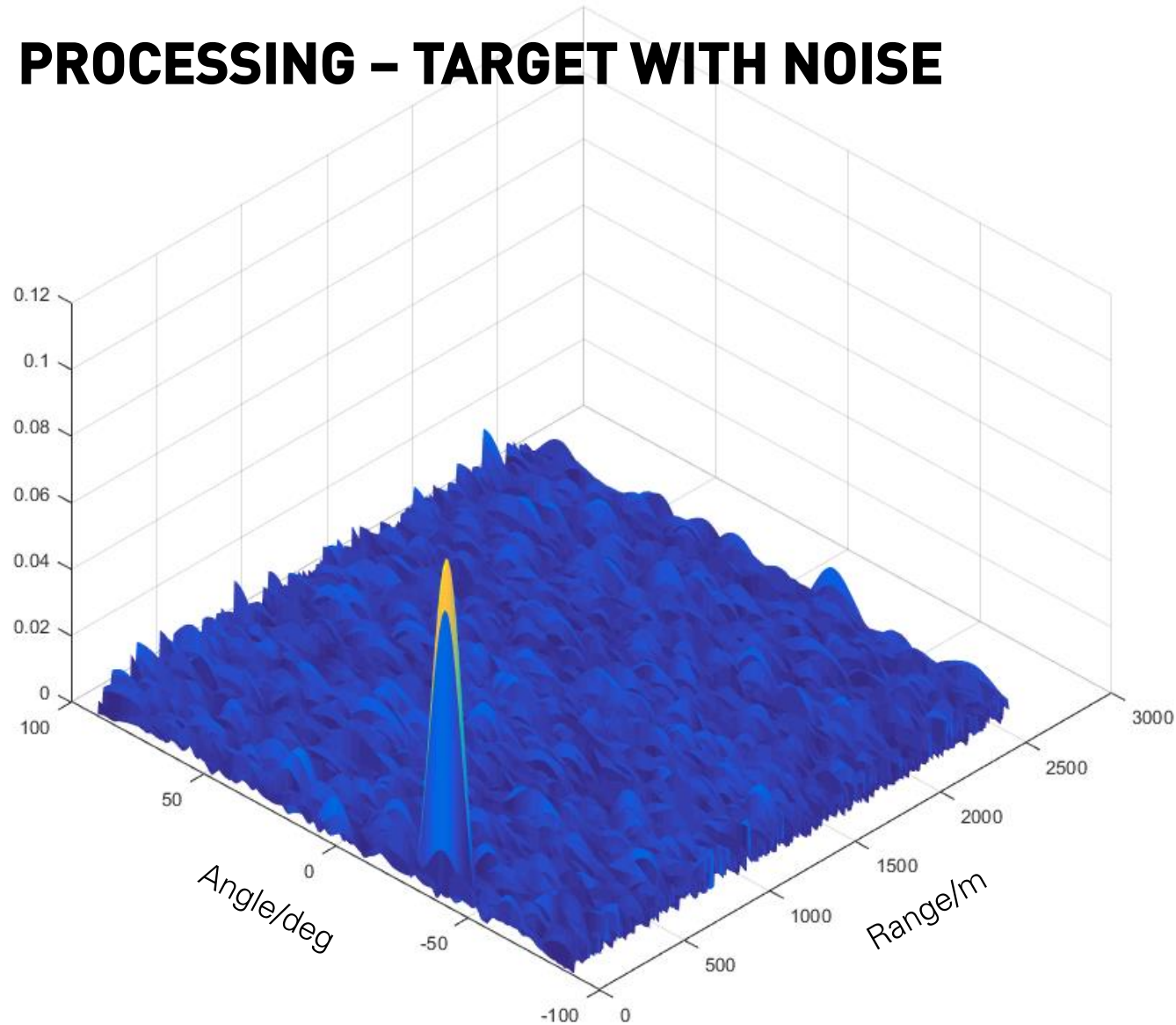
# PROCESSING – RADAR CUBE



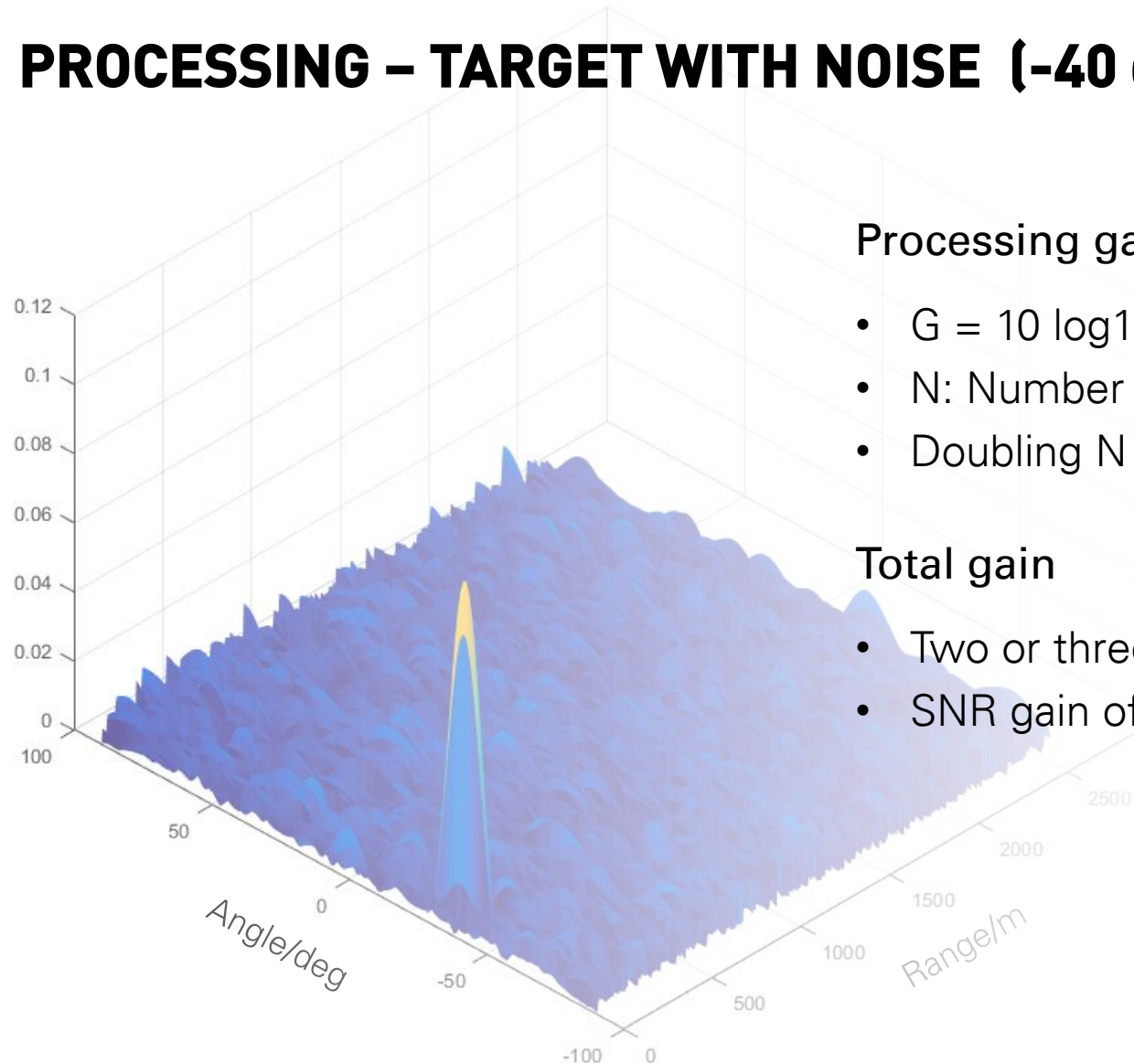
## 3D Memory arrangement

- Range – individual chirps
- Velocity – chirp sequence
- Angle – virtual elements

# PROCESSING – TARGET WITH NOISE



# PROCESSING – TARGET WITH NOISE (-40 dB SNR)



## Processing gain

- $G = 10 \log_{10} (N/2)$
- N: Number of samples
- Doubling N adds 3 dB SNR

## Total gain

- Two or three FFT stages
- SNR gain of 80 dB is possible

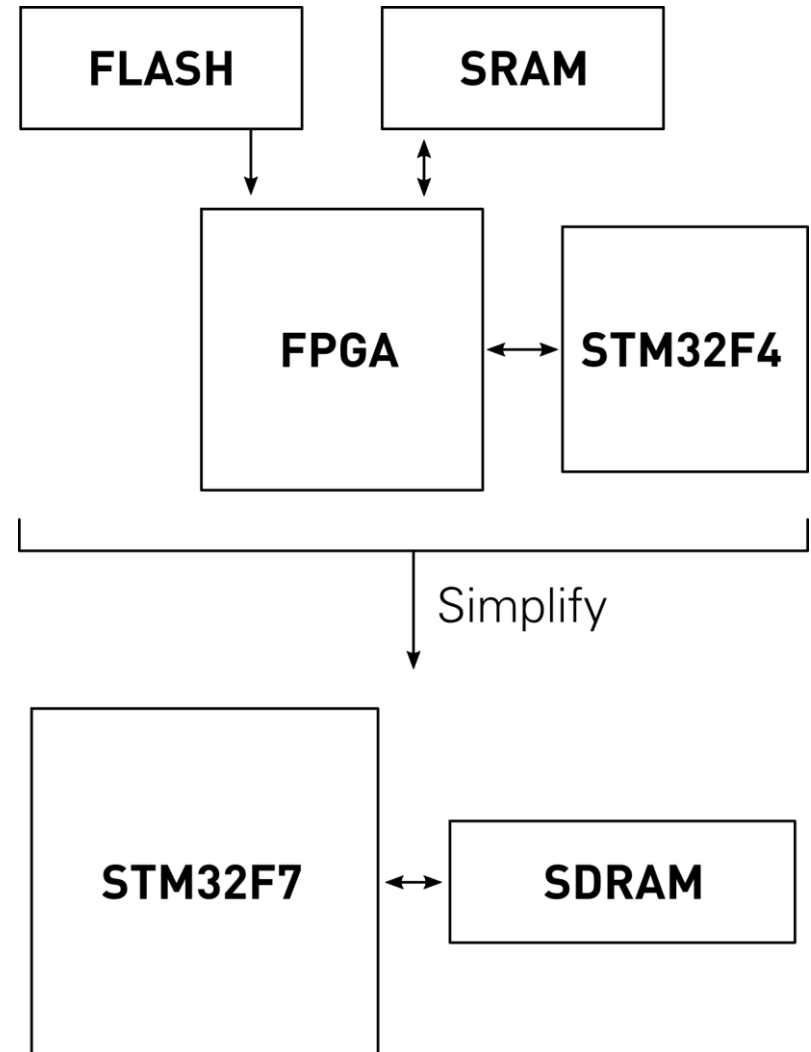
# SYSTEM DESIGN

## Simplification

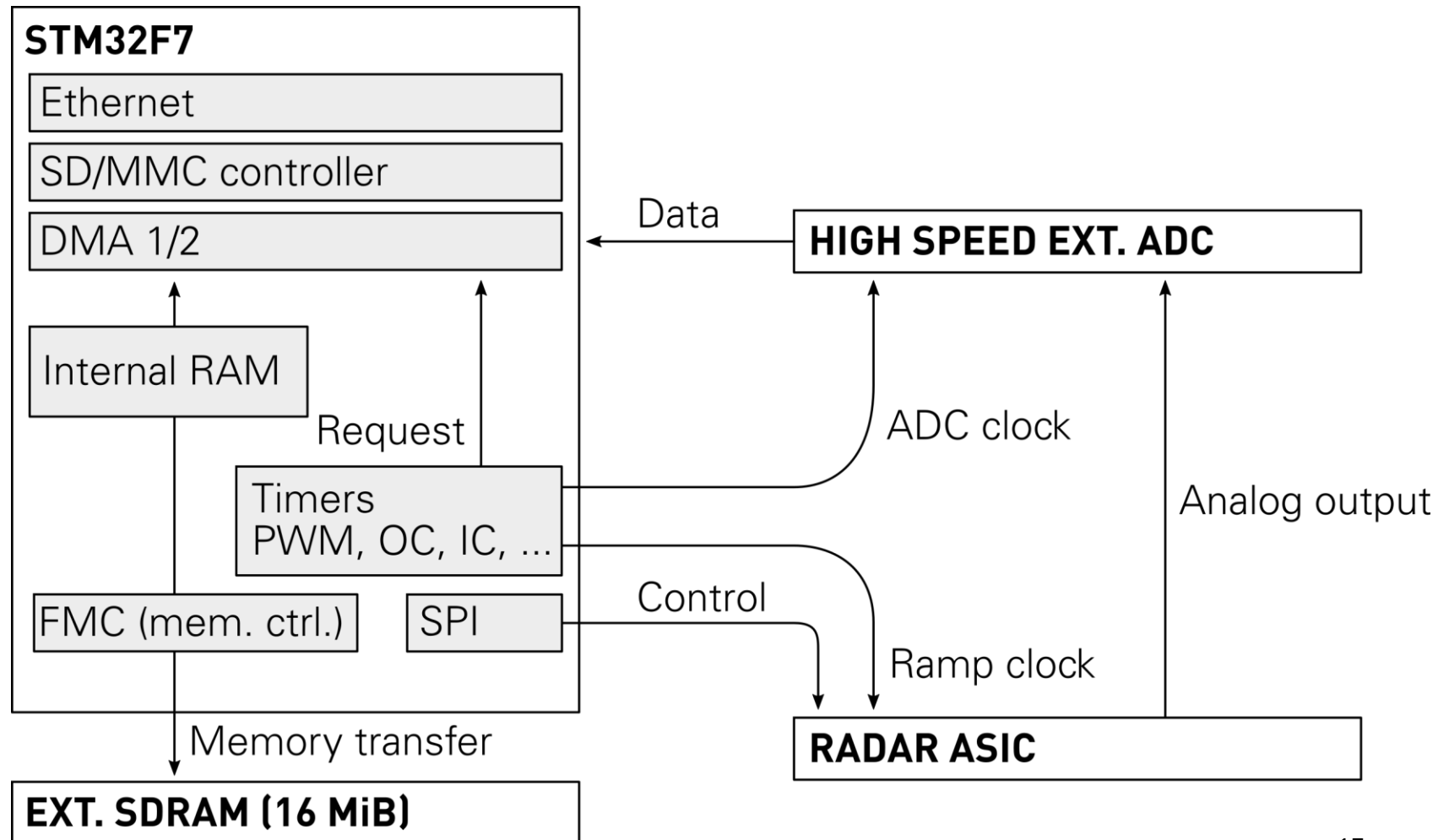
- Merge functions of FPGA and microcontroller
- Single application for all nodes

## Speedup

- Use of DMA, interrupts and double buffering for fast acquisition and processing
- Real time radar imaging
- Direct access to SDRAM



# SYSTEM DESIGN – BLOCK DIAGRAM



# ACHIEVEMENTS AND OUTLOOK

Evaluation of processing algorithms in Matlab

First implementation of primary radar

- Clock generation for ADC and PLL
- DMA access for ADC and transfer to storage
- External trigger for synchronous ramping
- No CPU load

Next steps

- Digital board design
- Implementation of processing algorithms
- Expand to MIMO



